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10/718,283	11/19/2003	Bo Huang	10559-886001	1064

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EXAMINER	
DARE, RYAN A	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,283	HUANG ET AL.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed March 2, 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. Included with the IDS were EPO 0742518A2 and WO 00/22513, which were considered. China Patent 1138175 was not included with the IDS and has thus not been considered.

Claim Objections

1. Claims 10-12 are objected to because of the following informalities: They recite the term "memory bank". The Examiner believes Applicant intends this term to be replaced with "memory bank", as in claims 7-9, and has been treated as such for the remainder of this Office Action. Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 27-30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The computer program product of claims 27-

30 is embodied in an information carrier, which could mean non-statutory electronic signals, and does not limit the scope of the claims to a statutory computer storage medium.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 11-18, and 23-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Pentkovski et al., US Patent 6,356,270.

3. With respect to claim 1, Pentkovski et al. teach a method comprising:

converting memory access instructions in a source code into a standard format, in fig. 5, where store or load commands that address consecutive locations in memory are first put in order in intermediate buffer 362 and combined in the write combining buffers 470.

generating partitions containing formatted memory access instructions, in fig. 5, reference characters W0, W1, W2 and W3.

generating a match set, the match set including matches of instruction patterns to the formatted memory access instructions in the partitions, in fig. 5, intermediate buffer 362, where, for example, store E0, E1, E2 and E3 form a match set.

transforming the matches to vector memory access instructions, in fig. 5, reference numeral 650, where store E0, E1, E2 and E3 are combined into one memory access instruction W0. See the related discussion in col. 6, lines 38-54.

4. With respect to claim 2, Pentkovski et al. teach the method of claim 1 in which converting comprises converting memory access instructions that read or write less than a minimum data access unit (MDAU) to memory access instructions that read or write a multiple of the minimum data access unit, in col. 1, lines 49-55. In a preferred embodiment, such as fig. 5, the MDAU is the size of one load or store, and four load or stores are combined into one memory access instruction.

5. With respect to claim 3, Pentkovski et al. teach the method of claim 2 in which converting further comprises transforming the memory access instructions that read or write the multiple of the minimum data access unit to a format including a base address plus an offset, in fig. 5, which puts, for example, store E0, E1, E2 and E3 in consecutive locations. It is disclosed that these locations are adjacent in col. 6, lines 26-33. As can be seen in the figure, the locations E0, E1, E2 and E3 comprise a base address at E0 and an offset that incorporates the consecutive memory locations through E3.

6. With respect to claim 4, Pentkovski et al. teach the method of claim 1 in which generating partitions comprises:

generating a data flow graph containing basic blocks including the memory access instructions, in fig. 5, where store or load commands are grouped together in intermediate buffer 362 and write combining buffers 470; and

for each basic block, applying a set of rules, in fig. 5.

7. With respect to claim 5, Pentkovski et al. teach the method of claim 4 in which applying comprises limiting a subnode of a partition to memory access instructions directed to a specific memory bank, in fig. 5, where the memory access instructions directed towards the E memory bank are put in the block W0.

8. With respect to claim 6, Pentkovski et al. teach the method of claim 5 in which applying further comprises limiting the subnode of a partition to a memory read or a memory write, in col. 1, lines 58-59.

9. With respect to claim 11, Pentkovski et al. teach the method of claim 5 in which the memory bank is flash memory, in col.3, line 29.

10. With respect to claim 12, Pentkovski et al. teach the method of claim 5 in which the memory bank is a NVRAM in col. 3, lines 26-30. Pentkovski et al. discloses flash memory, which is a specific type of NVRAM.

11. With respect to claim 13, Pentkovski et al. teach the method of claim 1 in which the instruction patterns comprise a pattern describing instruction semantics, in fig. 5. numeral 460.

12. With respect to claim 14, Pentkovski et al. teach the method of claim 1 in which the vector memory access instructions comprise single memory access instructions representing multiple memory access to a type of memory, as shown in fig. 5, where single memory access instructions such as store E0, E1, E2 and E3 are converted a to a single memory access instruction W0.

13. With respect to claim 15, Pentkovski et al. teach a compilation method comprising:

converting memory access instructions that read or write less than a minimum data access unit (MDAU) to memory access instructions that read or write a multiple of the minimum data access unit, in col. 1, lines 49-55. In a preferred embodiment, such as fig. 5, the MDAU is the size of one load or store, and four load or stores are combined into one memory access instruction.

converting the memory access instructions into a format including a base address plus an offset, in fig. 5, which puts, for example, store E0, E1, E2 and E3 in consecutive locations. It is disclosed that these locations are adjacent in col. 6, lines 26-33. As can be seen in the figure, the locations E0, E1, E2 and E3 have a base address at E0 and an offset that incorporates the consecutive memory locations through E3.

grouping subsets of the converted memory access instructions into partitions, in fig. 5, reference characters W0, W1, W2 and W3.

vectorizing the converted memory access instructions in the subsets that match instruction patterns, in fig. 5, reference numeral 650, where store E0, E1, E2 and E3 are combined into one memory access instruction W0. See the related discussion in col. 6, lines 38-54.

14. With respect to claim 16, Pentkovski et al. teach the compilation method of claim 14 in which grouping comprises:

generating a data flow graph containing basic blocks including memory access instructions, in fig. 5, where store or load commands are grouped together in intermediate buffer 362 and write combining buffers 470; and

generating subnodes in partitions, the subnodes including memory access instructions directed to a memory bank and performing the same operation, in fig. 5, where the memory access instructions directed towards the E memory bank are put in the block W0.

15. With respect to claim 17, Pentkovski et al. teach the compilation method of claim 16 in which the operation is a read, in col. 1, lines 58-59.

16. With respect to claim 18, Pentkovski et al. teach the compilation method of claim 16 in which the operation is a write, in col. 1, lines 58-59.

17. With respect to claim 23, Pentkovski et al. teach the method of claim 16 in which the memory bank is flash memory, in col.3, line 29.

18. With respect to claim 24, Pentkovski et al. teach the method of claim 16 in which the memory bank is a NVRAM in col. 3, lines 26-30. Pentkovski et al. discloses flash memory, which is a specific type of NVRAM.

19. With respect to claim 25, Pentkovski et al. teach the compilation method of claim 15 in which the instruction patterns comprises instruction semantics, in fig. 5. numeral 460.

20. With respect to claim 26, Pentkovski et al. teach the compilation method of claim 25 in which the instruction semantics comprises segments, in fig. 5, where W0 is split into 4 segments.

21. With respect to claims 27, 28, and 29, Applicant claims a computer program product that performs the method of claim 1, 2 and 3, respectively, and are therefore rejected using similar logic.

22. With respect to claim 30, Applicant claims the computer program product of claim 27, embodying the compilation method of claim 16, and is therefore rejected using similar logic.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

25. Claims 7-10 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pentkovski et al. as applied to claims 1-6 above, in view of the Microsoft Press Computer Dictionary, hereafter Microsoft.

26. With respect to claim 7, Pentkovski et al. teach all parent claims as discussed above, and also teaches that the memory can be a RAM, but fails to expressly teach that the memory can be an SRAM.

27. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the invention using an SRAM. It is widely known in the art that a RAM can either be a static RAM or a dynamic RAM. It would be obvious for a skilled artisan to use a SRAM to avoid the performance penalties associated with a dynamic RAM. Dynamic RAM's must constantly be refreshed, which creates wait states, thus making DRAM slower than SRAM, as taught by Microsoft on page 166, under the definition for dynamic RAM.

28. With respect to claim 8, Pentkovski et al. teach all parent claims as discussed above, and also teaches that the memory can be a RAM, but fails to expressly teach that the memory can be a DRAM.

29. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the invention using a DRAM. It is widely known in the art that a RAM can either be a static RAM or a dynamic RAM. It would be obvious for a skilled artisan to use a DRAM because dynamic RAMs circuitry is simpler and because they can hold up to four times as much data, as taught by Microsoft on page 166, under the definition for dynamic RAM.

30. With respect to claim 9, Pentkovski et al. teach all parent claims as discussed above, but fails to expressly teach that the memory can be a scratchpad memory.

31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the invention using a scratchpad memory because a scratchpad memory is high-speed, thus allowing for rapid retrieval of small items of data, as taught by Microsoft on page 421, under the definition of scratchpad.

32. With respect to claim 10, Pentkovski et al. teach all parent claims as discussed above, but fails to expressly teach that the memory can be an EEPROM.

33. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the invention using an EEPROM because it is useful for stable storage of data for long periods without electricity while still allowing reprogramming, as taught by Microsoft on page 170.

34. With respects to claims 19, 20, 21 and 22, Pentkovski et al. teach the limitations of all parent claims as discussed supra, and are rejected using similar logic as claims 7, 8, 9 and 10 above, respectively.

Conclusion

1. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar memory access instruction vectorization methods.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
December 22, 2005

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